CLAIMS:

1. A method for configuring a regulator circuit having a sample-and-hold circuit, comprising:

coupling an input voltage to an input node of the sample-and-hold circuit;

activating the sample-and hold circuit in response to the input voltage;

sensing an output voltage at an output node coupled to the sample and hold circuit;

determining whether the input voltage at the input node is greater than the output voltage at the output node; and

providing a sample-and-hold function based on the determination.

2. The method of claim 1 wherein a transfer function of the sample-and-hold circuit is pseudo-all-pass if the input voltage at the input node is greater than an output voltage at the output node and is a substantially constant signal if the input voltage at the input node is less than the output voltage at the output node.

3. The method of claim 2 wherein the regulator circuit comprises a buck-boost converter, a differential amplifier, a PID controller, a sample-and-hold circuit and a PWM modulator.

4. The method of claim 2 wherein the sample-and-hold circuit is passive.

5. The method of claim 4 wherein the sample-and hold circuit comprises a series input resistor coupled to an input of a forward biased diode wherein the output of the diode is coupled to a capacitor in parallel with a resistor shunted to ground wherein the output of the sample-and-hold is taken from the output of the diode.

6. The method of claim 5 wherein providing the sample-and-hold circuit transfer function comprises arranging a first pass diode coupled between the input node and the output node and a second pass diode coupled between the sample-and-hold circuit and the output node.

7. The method of claim 6 wherein the first pass diode and the second pass diode are sensing the output voltage at the output node.

8. The method of claim 2 wherein coupling the input voltage to the sample-and-hold circuit comprises coupling the output of the differential amplifier wherein the differential amplifier is arranged to sense current through an LED.

9. The method of claim 2 wherein activating the sample-and hold circuit in response to the input voltage comprises energizing the sample-and-hold circuit with the voltage signal.

10. The method of claim 1 wherein the regulator circuit is capable of DC operation and low-frequency PWM current drive of LEDs.

11. A regulator circuit having a sample-and-hold circuit, comprising:

a regulation circuit;

a sample-and-hold circuit coupled to input and output nodes wherein the input node and output node are coupled to the regulation circuit; and

wherein a transfer function of the sample-and-hold circuit is pseudo-all-pass if the input voltage at the input node is greater than an output voltage at the output node and is a substantially constant signal if the input voltage at the input node is less than the output voltage at the output node.

12. The regulator circuit of claim 11 wherein the sample and hold circuit further comprises a first pass diode coupled between the input node and the output node and a second pass diode coupled between the sample-and-hold circuit and the output node.

13. The regulator circuit of claim 12 wherein the regulation circuit is capable of DC operation and low-frequency PWM current drive of LEDs.

14. The regulator circuit of claim 12 wherein the regulation circuit comprises a buck-boost converter, a differential amplifier, a PID controller, a sample-and-hold circuit and a PWM modulator.

15. The regulator circuit of claim 14 wherein the sample-and-hold circuit is passive.

16. The regulator circuit of claim 15 wherein the sample-and hold circuit comprises a series input resistor coupled to an input of a forward biased diode wherein the output of the diode is coupled to a capacitor in parallel with a resistor both shunted to ground wherein the output of the sample-and-hold circuit is taken from the output of the diode.

17. The regulator circuit of claim 16 wherein the first pass diode and the second pass diode are forward biased from the input node to the output node.

18. A system for configuring a regulator circuit having a sample-and-hold circuit, comprising:

means for coupling an input voltage to an input node of the sample-and-hold circuit;

means for activating the sample-and hold circuit in response to the input voltage;

means for sensing an output voltage at an output node coupled to the sample and hold circuit;

means for determining whether the input voltage at the input node is greater than the output voltage at the output node; and

means for providing a sample-and-hold function based the determination.